# Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASSCHE

*Abstract*—A novel way to obtain a very high accuracy in the bit weighting required for monolithic digital-to-analog (D/A) converters will be described. The new method combines passive division using matched elements with a time division concept, needs no trimming, and is insensitive to element aging. A 12-bit monolithic D/A network with internal reference sources, built as a test circuit, demonstrates the versatility of this new technique.

## Introduction

MONOLITHIC D/A converters have received considerable attention due to the rapidly expanding digital signal processing and microprocessor markets. Although there are numerous approaches to obtain a high-performance D/A converter, circuit design has settled down around the $R$-$2R$ ladder network to obtain the required precision in binary weighting of current sources. Here the designer makes use of the excellent matching characteristics and thermal tracking of integrated components. The accuracy of the converter is determined by the matching of the $R$-$2R$ resistors and of the current source transistors. Using no trimming techniques, a 10-bit D/A converter can be designed having $\frac{1}{2}$LSB linearity but circuit yield in production is troublesome. Laser trimming techniques are therefore used to improve yield.

Converters based on time division, such as pulsewidth modulators, for example, require no trimming and have a high accuracy. The main disadvantage of these converters is the low conversion speed due to the high degree of filtering required to reduce the ripple on the output signal. To break through the barrier of 10-bit accuracy to achieve 12-, 14-, or in the near future, even 16-bit accuracy in a monolithic form, a new design procedure is required. A proposal will be described here which basically combines passive division using matched elements with a time division method [1]. This method allows high accuracy without trimming in a standard IC process. A 12-bit D/A network built as a test circuit will be described to demonstrate the versatility of this new technique.

## Standard Monolithic Circuit Approaches

A circuit diagram of the three most significant bits of an $R$-$2R$ ladder network D/A converter is shown in Fig. 1(a). The conversion takes place by summing the collector currents of $T_1$, $T_2$, and $T_3$ through the digitally controlled switches $S_1$, $S_2$, and $S_3$. The binary weighting of the currents through $T_1$, $T_2$, and $T_3$ requires a scaling of the emitter geometries resulting in equal base-emitter voltages of these transistors.

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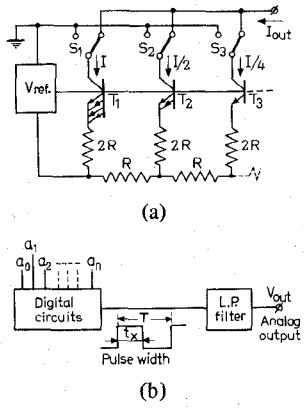



Fig. 1. (a) Binary weighted currents using an $R$-$2R$ ladder network. (b) Pulsewidth modulation D/A converter.

TABLE I
Comparison of Three Different Resistor Fabrication Processes

| Fab. process | Matching tolerance | | | |
|---|---|---|---|---|
| | σ(%) | | mean(%) | |
| | 10μ | 40μ | 10μ | 40μ |
| Diffusion | 0.44 | 0.23 | −0.1 | 0.07 |
| Thin film | 0.24 | 0.11 | −0.1 | −0.06 |
| Ion implant | 0.34 | 0.12 | 0.05 | 0.05 |

The matching characteristics of the $R$-$2R$ resistors in the ladder network and of the base-emitter voltages of transistors $T_1$, $T_2$, and $T_3$ determine the overall accuracy of the converter.

Three different resistor fabrication techniques are available to the designer as shown in Table I [2]. The data in the column giving the standard deviation for resistors with a linewidth of 10 μm and 40 μm show that 10-bit converters with $\frac{1}{2}$LSB linearity can be fabricated although production yield will be low. A simplified form of a pulsewidth modulator D/A converter is shown in Fig. 1(b). In the digital circuitry a function is performed giving an output voltage equal to $V_{\text{ref}}$ for a time $T_x$ which is proportional to the digital input signals $a_0$ to $a_n$ and zero for the remaining time of the period $T$. The low-pass filter averages the pulsewidth-modulated signal resulting in the output voltage $V_{\text{out}} = (T_x/T) \cdot V_{\text{ref}}$. A high degree of filtering is required to reduce the ripple on the output voltage below the required level. The low overall speed of these converter types is a big disadvantage.

## New Divider Circuit

The basic scheme of the new divider circuit is shown in Fig. 2(a). It consists of a passive current divider and a set of switches driven by the clock generator $f$. The total current $2I$ is divided by the passive current divider into two nearly

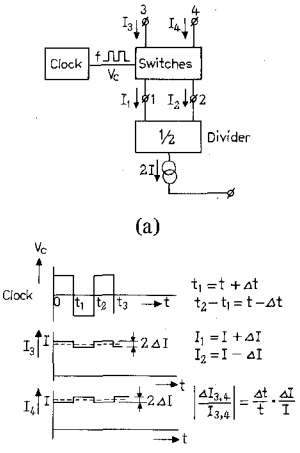



Fig. 2. (a) New current divider schematic diagram. (b) Time dependence of various currents in the new divider.

equal parts: $I_1 = I + \Delta I$ and $I_2 = I - \Delta I$. The currents $I_1$ and $I_2$ are now interchanged for equal time intervals with respect to the output terminals 3 and 4. At the output terminals currents will then flow whereby the *average values* are exactly equal and have a dc value equal to $I$. Fig. 2(b) shows the currents as a function of time. A small ripple current $2\Delta I$ of a frequency $f$ is present on the output currents too. This ripple is a measure for the matching performance of the passive divide-by-two stage. With a simple low-pass filter this small ripple current can be suppressed below the required value and an *exact* 1 to 2 current ratio is obtained without using any *accurate element*. If the time intervals during which the currents $I_1$ and $I_2$ are interchanged differ by a value $\Delta t$ [see Fig. 2(b)], there is an error in the 1 to 2 division equal to

$$\frac{\Delta I_{3,4}}{I_{3,4}} = \frac{\Delta t}{t} \cdot \frac{\Delta I}{I}.$$

The total error is the product of two small errors, resulting in a very high overall accuracy. It is not difficult in practice to make $\Delta t/t \leqq 0.1$ percent and $\Delta I/I \leqq 5$ percent, so an overall accuracy better than $5 \times 10^{-5}$ can easily be obtained using this division stage. The value of the ripple can be reduced by optimizing the matching characteristics of the passive divide-by-two stage. This reduction of the ripple allows the use of a simple low-pass filter network consisting of only one *RC* network.

Generally speaking: *dynamic element matching* can be used advantageously in those cases where a network consists of or can be divided into a number of nearly equal elements. An improvement in overall accuracy can be obtained by a continuous and cyclic interchange of these nearly equal elements. The average value of the output signals is a few orders of magnitude more accurate then the accuracy of the basic network.

## Practical Divider Circuit

The practical divider circuit is shown in Fig. 3. The current mirror $T_1$, $T_2$ performs the passive division of the total current $2I$ into two nearly equal parts. Two Darlington differential

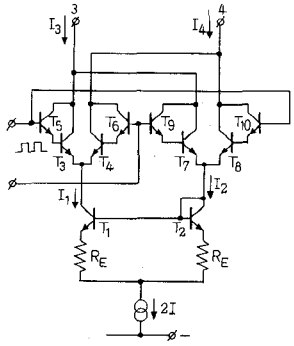



Fig. 3. Practical current divider stage.

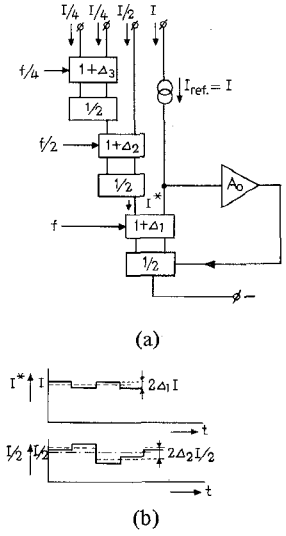



Fig. 4. (a) Binary weighted current network using different switching frequencies. (b) Time dependence of currents flowing in the first and second divider stage.

stages ($T_3$ to $T_{10}$) interchange the currents $I_1$ and $I_2$ for equal time intervals between the output terminals 3 and 4. The already discussed improvement in division accuracy with respect to the current mirror is now found. In practice the base currents of the Darlington switches limit the division accuracy. The *only* criterion determining the overall accuracy for the *whole circuit* is a high current gain (e.g., $\beta^2 > 10^4$) for the switching transistors. This is not such a big problem while, if necessary, a special high current gain process for the transistor fabrication can be used. The value of the ripple depends on the matching characteristics of the current mirror transistors $T_1$ and $T_2$. This matching can be improved by inserting emitter degeneration resistors across which a voltage drop of about $\frac{1}{4}$ to $\frac{1}{2}$ V is needed for an optimum matching performance. According to Table I a matching better than 0.5 percent for the currents $I_1$ and $I_2$ can be obtained with a reasonable circuit yield. This results in a ripple current $\leqq 0.5$ percent $I$. No accurate elements are used and aging of elements has no influence on the overall accuracy.

## Binary Weighted Current Network

A binary weighted current network is formed by cascading current-division elements [see Fig. 4(a)]. In the first divider

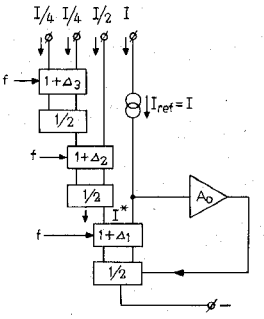
stage a combination with a reference current source $I_{ref}$ and a current amplifier $A_0$ is used as an accurate current mirror. This mirror circuit will be described later. To avoid interactions between the individual divider stages the switching frequencies are halved for every following divider stage. In Fig. 4(b) the output currents of the first two stages are shown as a function of time. That no interaction occurs can be explained as follows. The current $I^*$ shows the inaccuracy $\Delta_1$ of the first divider stage [upper diagram of Fig. 4(b)]. In the output current $I/2$ of the second divider stage we can distinguish the error $\Delta_2$ with the frequency $f/2$ and the error $\Delta_1$ of the first stage with a frequency $f$ [lower diagram of Fig. 4(b)]. During a half-period of the $f/2$ clock the average value of the current $I/2$ does not contain an error term originating from the first divider stage of frequency $f$. This means that over the total period of the $f/2$ clock no interactions from the first divider stage are found. An independent operation of the stages is thus indeed obtained.

The disadvantages of halving the switching frequencies are found to be a large increase of the digital circuitry for the generation of the different clock signals and a more difficult suppression of ripple due to the reduction in frequency. Another solution with switches operating at the same frequency is therefore used.

## Current Network with One Switching Frequency

A binary weighted current network with every individual divider stage operating at the same frequency $f$ is shown in Fig. 5. Now the interactions between individual stages must be taken into account. For the error in the first divider stage we may take the same result as obtained in the calculations in Fig. 2. This will be proved in the next section.

Because the time errors are the same for all the divider stages they can be separated from the stage errors. The error term of the second stage ($I/2$) can then be calculated with: $0 - t_1 = t + \Delta t$ and $t_2 - t_1 = t - \Delta t$. The average value for the output current $I/2$ becomes




(a)

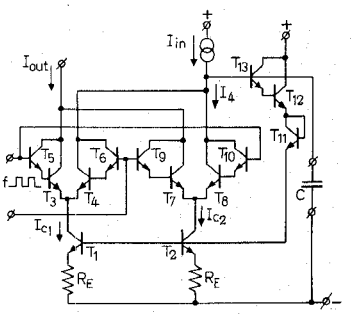
$$I^* = I_{ref}\left(1+\Delta_1\cdot\frac{\Delta t}{t}\right)$$

$$I/2 = \frac{I_{ref}}{2}\left[1+\Delta_1\cdot\Delta_2+(\Delta_1+\Delta_2)\cdot\frac{\Delta t}{t}\right]$$

$$I/4 = \frac{I_{ref}}{4}\left[1-\Delta_1\Delta_2+\Delta_1\Delta_3-\Delta_2\Delta_3+(\Delta_1-\Delta_2+\Delta_3)\cdot\frac{\Delta t}{t}\right]$$

(b)

Fig. 5. (a) Binary weighted current network with equal switching frequency. (b) Error analysis results.




(a)

With Cap. C: $\bar{I}_4 = I_{in}$

$\bar{I}_{out} = I_{in}$

Without Cap. C: $I_{C_1} = I_{C_2}(1+\Delta)$

$0 - t_1: I_{out} = I_{in}(1+\Delta)$

$t_1 - t_2: I_{out} = \frac{I_{in}}{1+\Delta} \cong I_{in}(1-\Delta+\Delta^2)$ if $\Delta \ll 1$

$\Delta \leq 0.5\%$ with $R_E \Rightarrow \frac{\bar{I}_{out} - I_{in}}{I_{in}} \cong \frac{\Delta^2}{2} \ll 10^{-4}$

(b)

Fig. 6. (a) Accurate current mirror. (b) Error analysis results.

$$\overline{I/2} = \frac{I_{ref}(1+\Delta_1)\frac{1}{2}(1+\Delta_2)(t+\Delta t) + I_{ref}(1-\Delta_1)\frac{1}{2}(1-\Delta_2)(t-\Delta t)}{2t}$$

$$\overline{I/2} = \frac{I_{ref}}{2}\left[1+\Delta_1\Delta_2+(\Delta_1+\Delta_2)\frac{\Delta t}{t}\right]$$

which results in an error term equal to: $\Delta_1\Delta_2 + (\Delta_1 + \Delta_2)\cdot(\Delta t/t)$.

If the error terms of the individual stages are made small ($\Delta_{1\to n} \leqq 0.5$ percent), then the influence of the interactions between the individual divider stages on the overall accuracy of the D/A network can be kept very low. If averaging capacitors are applied between subsequent current dividers all $\Delta_i\Delta_j$ errors due to interaction would be removed.

In Fig. 5(b) the result of the calculations for the first three most important bits is shown. Although an increase of error terms is found with a rising number of the divider stage (e.g., the $I/4$ error term is $-\Delta_1\Delta_2 + \Delta_1\Delta_3 - \Delta_2\Delta_3$) this increase can be tolerated because in the overall performance a reduction of this error is found proportional to the bit weight ($I_{ref}/N$). Now the frequency of the error ripple is the same for all the output currents and can be chosen high to simplify the filtering. A small $RC$ low-pass filter can be incorporated in every switched output terminal. An identical behavior for the new circuit and a very well-trimmed ladder network D/A converter is then found.

## Accurate Current Mirror

A detailed circuit diagram of the accurate current mirror is shown in Fig. 6. The basic current mirror consists of the current sources $T_1$ and $T_2$ with the Darlington stage $T_{12}T_{13}$ to form the feedback loop. The Darlington differential stages

TABLE II
ERROR TERMS OF 3-BIT D/A CONVERTER

| | ERROR TERMS OF 3 BIT DAC | |
|---|---|---|
| Bit | With Cap C | Without Cap C |
| $I^*/I$ | $1+\Delta_1\cdot\frac{\Delta t}{t}$ | $1-\frac{1}{2}\Delta_1^2+\Delta_1\cdot\frac{\Delta t}{t}$ |
| $I/2I$ | $1+\Delta_1\Delta_2+(\Delta_1+\Delta_2)\cdot\frac{\Delta t}{t}$ | $1+\Delta_1\Delta_2+\frac{1}{2}\Delta_1^2+(\Delta_1+\Delta_2)\cdot\frac{\Delta t}{t}$ |
| $I/4I$ | $1-\Delta_1\Delta_2+\Delta_1\Delta_3-\Delta_2\Delta_3+(\Delta_1-\Delta_2+\Delta_3)\cdot\frac{\Delta t}{t}$ | $1-\Delta_1\Delta_2+\Delta_1\Delta_3-\Delta_2\Delta_3+\frac{1}{2}\Delta_1^2+(\Delta_1-\Delta_2+\Delta_3)\cdot\frac{\Delta t}{t}$ |

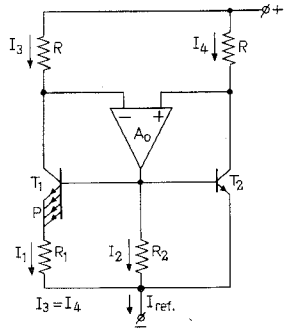



Fig. 7. Schematic diagram of the current reference source.

$T_3$ to $T_{10}$ interchange for equal time intervals the currents $I_{c1}$ and $I_{c2}$ with respect to the summing point at the base of $T_{13}$. Two cases can now be distinguished.

1) An averaging capacitor $C$ is connected between the base terminal of $T_{13}$ and the negative supply. The average value of $I_{c1}$ and $I_{c2}$ being $\bar{I}_4$ is then made equal to $I_{\text{in}}$. Now because the average value $\bar{I}_{\text{out}}$ is equal to $\bar{I}_4$ as was shown earlier (Fig. 2), the complete circuit results in an accurate current mirror $\bar{I}_{\text{out}} = I_{\text{in}}$.

2) The capacitor $C$ is deleted. During the first half-period of the clock the current $I_{c2}$ is then made equal to $I_{\text{in}}$ resulting with an error $\Delta$ between the transistors $T_1$ and $T_2$ in an output current $I_{\text{out}} = I_{\text{in}}(1+\Delta)$. In the second half clock period $I_{c1}$ and $I_{c2}$ are interchanged so now $I_{\text{in}} = I_{c1}$ which results in an output current $I_{\text{out}} = I_{\text{in}}/1+\Delta$. If $\Delta$ is made small ($\Delta \ll 1$) then this division can be approximated by a finite expansion resulting in: $I_{\text{out}} \cong I_{\text{in}}(1-\Delta+\Delta^2)$. After averaging over the whole clock period we obtain $I_{\text{out}} \cong I_{\text{in}}(1+\frac{1}{2}\Delta^2)$. With $\Delta \leqq 0.5$ percent the error term can be kept very small ($\approx 10^{-5}$). Table II summarizes the results of the error calculations for a 3-bit network incorporating an accurate current mirror. Without the capacitor $C$ a slight decrease in overall accuracy is found.

## Current Reference Source

An important part of a D/A converter is the reference source. Because the whole converter operates with currents a *current* source was taken as a reference source. The simplified circuit diagram is shown in Fig. 7. If the resistor $R_2$ is deleted, the circuit behaves like a simple current stabilizer. The operation of the circuit is as follows. The resistors $R$ with the operational amplifier $A_0$ permit equal collector currents to flow through transistors $T_1$ and $T_2$. Transistor $T_1$ has a $p$ times larger emitter area than transistor $T_2$. A stable operation of the circuit will give a voltage drop across resistor $R_1$ in accordance with this difference in emitter area. Now the current through $T_1$ and $T_2$ can be calculated, resulting in

$$I_1 R_1 = \frac{kT}{q} \ln p \qquad (I_3 = I_4 = I_{c1} = I_{c2}).$$

The temperature coefficient of the current $I_1$, with temperature-independent resistors, can be calculated, yielding $(1/I_1)\cdot(\partial I_1/\partial T) = 1/T$. Now resistor $R_2$ is inserted. The current through $R_2$ is determined by the base-emitter voltage $V_{BE_2}$ of transistor $T_2$ so that $I_2 = V_{BE_2}/R_2$. The temperature coefficient of the current $I_2$ can be estimated resulting in

$$\frac{\partial I_2}{\partial T} \cong \frac{V_{BE_2} - V_g}{TR_2}$$

and, with

$$V_{BE_2} \approx \frac{1}{2} V_g, \qquad \frac{1}{I_2}\frac{\partial I_2}{\partial T} \approx -\frac{1}{T}$$

($V_g$ equals bandgap voltage of silicon).

The output current $I_{\text{ref}}$ is equal to the sum of $I_2 + 2I_1 = I_{\text{ref}}$. The temperature coefficient can be adjusted to zero at room temperature by choosing suitable values for $R_1$ and $R_2$. The temperature relation is based on the same principle as in the well-known bandgap voltage sources [3], [4]. Solving the temperature equations for the reference source, an independent equation for the resistor $R_2$ can be found. With $\partial I_{\text{ref}}/\partial T = 0$ at $T = T_0$ we obtain

$$R_2 = \frac{V_g + \dfrac{kT_0}{q}(n-1)}{I_{\text{ref}}}$$

with

$$n \approx 1.4$$

and

$$V_g = 1.205 \text{ V}.$$

With a desired value for $I_{\text{ref}}$ at $T = T_0$ the value of $R_2$ can be calculated. This value is used in the implicit equation for $I_1$ giving

$$2I_1 + \frac{kT_0}{qR_2} \ln \frac{I_1}{i_{02}} = I_{\text{ref}}.$$

Here $i_{02}$ is the base-emitter diode reverse current of transistor $T_2$ at $T = T_0$. Then $R_1$ can be calculated from

$$R_1 = \frac{kT_0}{qI_1} \ln p.$$

These equations are derived from a simplified model for the reference source.

## Practical Diagram of the Reference Current Source

The circuit diagram of the practical reference source is shown in Fig. 8. The operational amplifier consists of a differential stage $T_3$, $T_4$ with a p-n-p current mirror ($T_5$, $T_6$, $T_7$) as an active load and a Darlington stage $T_8$, $T_9$ as an output ampli-

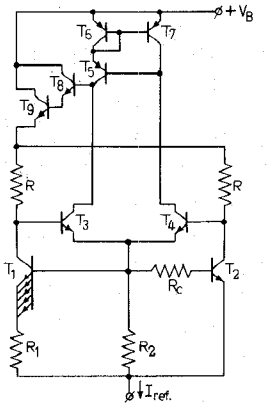



Fig. 8. Practical circuit diagram of the reference source.

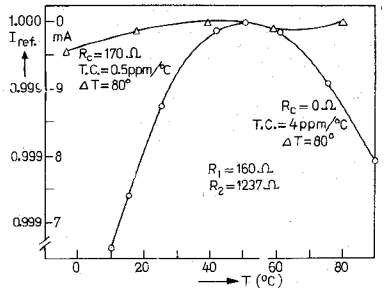



Fig. 9. Temperature measurements on the reference source.

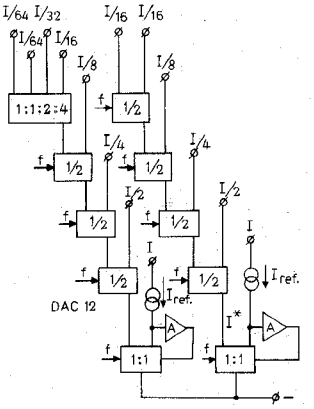



Fig. 10. Schematic diagram of complete 12-bit D/A converter.

fier. In this circuit an additional resistor $R_c$ is inserted which consists of a buried base resistor to compensate for the second-order term in the temperature equation. With an extended model and inserting temperature data for the resistor $R_c$, an optimum value at $I_{ref} = 1$ mA for $R_c$ of 170 Ω with $R_1 = 160$ Ω and $R_2 = 1237$ Ω is found. ($R_1$ and $R_2$ are off-chip resistors). This optimum for $R_c$ is rather flat so variations do not have a large influence on the overall temperature response. Temperature measurements are shown in Fig. 9. Without the compensation resistor $R_c$ the well-known parabolic relation with temperature is found, resulting in a temperature coefficient of 4 ppm/°C over $\Delta T = 80$°C. With the resistor $R_c$ inserted into the circuit, an improvement of about a factor of 10 is obtained giving a TC of 0.5 ppm/°C over $\Delta T = 80$°C.

At high temperatures (above 80°C) the substrate leakage currents of the transistors can no longer be ignored so an increase in the temperature coefficient is found.

## Schematic Diagram of 12-Bit Current Network

A schematic diagram of the complete 12-bit current network is shown in Fig. 10. A 5-bit high-accuracy divider with a reference source $I_{ref}$ can be distinguished. Furthermore a 7-bit less-accurate divider consisting of 4 bits using switched dividers and 3 bits using a passive division also with a reference source $I_{ref}$ completes the 12-bit network. Because both reference current sources are equal, an additional current divider to set the proper current relationship between the stages for the first 5 and last 7 bits is required. This current divider is applied after the digital input controlled bit current switching is performed and therefore not shown in Fig. 10.

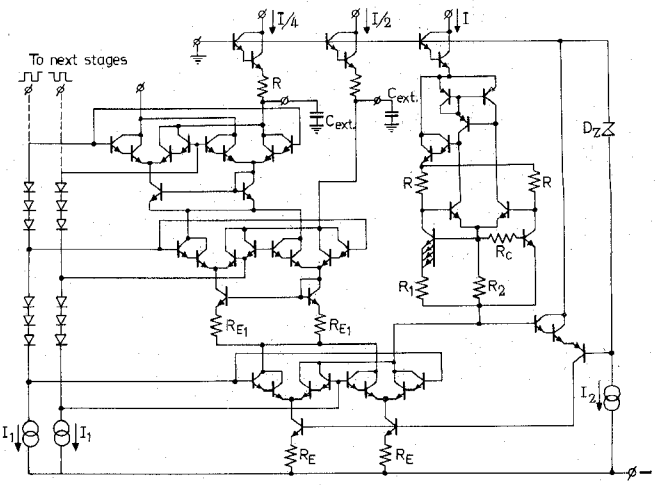



Fig. 11. Detailed circuit diagram of the three most significant bits.

An emitter-coupled multivibrator generates the clock frequency required for the dynamic matching procedure. A detailed circuit diagram of the three most significant bits and the reference source is shown in Fig. 11. Additional bonding pads

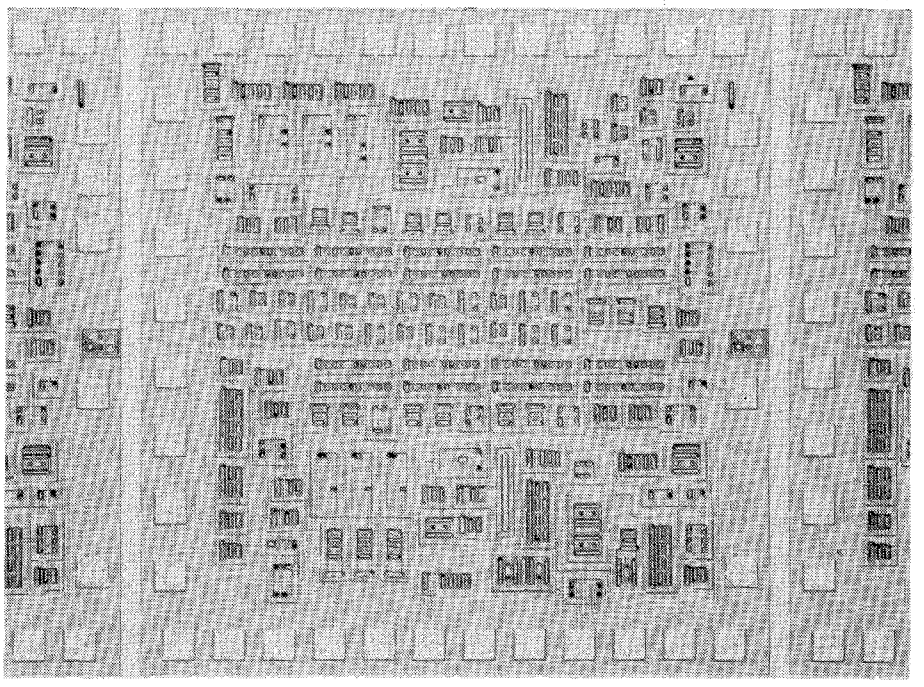


Fig. 12. Photomicrograph of the test chip.

TABLE III
PERFORMANCE CHARACTERISTICS OF THE MONOLITHIC 12-BIT D/A TEST CHIP

| D/A NETWORK DATA | |
|---|---|
| Resolution: | 12 bit |
| Accuracy: | ≤¼ L.S.B. or $5 \cdot 10^{-5}$ (linearity) |
| Output current: | 2 mA |
| Temp. Coeff. of output current: | 5 ppm/°C |
| Voltage Coeff. of output current: | 1 ppm/V |
| Chip size: | 2.5 × 2.5 mm |
| Max. clock freq. for dynamic matching: | 100 kHz |
| Power supply: | −15V |

allow filtering of the ripple currents per bit with $C_{ext}$ if needed. High-speed applications are therefore possible too. In low-speed applications filtering at the output summing amplifier can be used, requiring only one capacitor. The voltage drop across the reference current source is stabilized by the Zener diode $D_Z$. In this way the sensitivity of the reference current to supply variations $[(1/I_{ref})(\partial I_{ref}/\partial V_B) \cong 10^{-4}/V]$, already low, is further improved. A photomicrograph of the test chip is shown in Fig. 12. Table III gives the results of measurements on these test chips.

## CONCLUSION

The dynamic element matching method gives a simple, accurate, and reliable design procedure for high-accuracy monolithic D/A converters. The method requires no trimming and is insensitive to process variations and aging of components. The high accuracy obtained in the test circuit shows promise that an increase in the number of bits will be possible. Using a special process combining MOS with bipolar transistors, a 16-bit monolithic converter appears to be on the horizon in the near future.

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